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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/224,756	01/04/1999	RICHARD PIERRE FOURNEL	S1022/8175	3287

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EXAMINER	
LOKE, STEVEN HO YIN	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 09/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/224,756	FOURNEL, RICHARD PIERRE	
	Examiner	Art Unit	
	Steven Loke	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 1 and 3-12 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 5, 6, 11 and 12 of U.S. Patent No. 6,144,078 (Fournel). Although the conflicting claims are not identical, they are not patentably distinct from each other because the present application and the Fournel patent disclose the similar claimed subject matters.

In regards to claim 1, Fournel discloses a method for programming a read-only memory cell including a transistor formed in a semiconductor substrate of a first doping type, the transistor having a drain and a source of a second doping type separated in the substrate by a conduction channel, the method comprising a step of (claim 11, lines 1-7 of Fournel): contradoping a first region of the source such that the first region is of the first doping type to prevent a transistor effect from occurring, the first region directly contacting the conduction channel (claim 11, lines 8-12 of Fournel); wherein the step of contradoping includes a step of contradoping only the first region of the source of the transistor such that a second region of the source remains of the second doping type

(claim 11, lines 15-22 of Fournel); and wherein the second region has a lower doping concentration than the drain of the transistor (claim 12 of Fournel).

In regards to claim 3, Fournel discloses a memory, in integrated circuit form, comprising: a plurality of cells including a memory cell, wherein the memory cell has a drain and a source separated by a conduction channel, wherein the conduction channel and a first region of the source of the transistor directly contact each other and wherein the first region is contradoped so that the first region and the conduction channel are of the same doping type, and wherein the drain is not contradoped (claim 5, lines 1-10 of Fournel); wherein a second region of the source has a lower doping concentration than the drain of the transistor (claim 6 of Fournel).

Fournel differs from the claimed invention by not showing a plurality of transistors that form a corresponding plurality of memory cells, wherein each transistor has a drain and a source separated by a conduction channel.

It would have been obvious to have a plurality of transistors that form a corresponding plurality of memory cells, wherein each transistor has a drain and a source separated by a conduction channel because transistors are widely used memory cell structure in an integrated circuit memory.

In regards to claim 4, Fournel further discloses the drain and the second region of the source of the transistor are of the same doping type (claim 5, lines 1-13 of Fournel).

In regards to claim 12, Fournel further inherently discloses the first region is originally of a doping type that is opposite that of the conduction channel (claim 5, lines 1-10 of Fournel) because there are only two doping types in a semiconductor device.

In regards to claim 5, Fournel discloses a memory, comprising: a plurality of cells formed in a substrate of a first doping type, the plurality of cells including a first programmed cell having a drain of a second doping type, a conduction channel of the first doping type, and a source, wherein the source includes a first region of the first doping type directly contacting the conduction channel (claim 5, lines 1-10 of Fournel); wherein a second region of the source has a lower doping concentration than the drain (claim 6 of Fournel); and wherein the first region is the only region of the source that is contradoped (claim 5, lines 1-10 of Fournel).

In regards to claim 6, Fournel further discloses the second region is of the second doping type and contacts the first region (claim 5, lines 11-13 of Fournel).

In regards to claim 7, Fournel discloses a memory, comprising: a plurality of cells formed in a substrate of a first doping type, the plurality of cells including a first programmed cell having a drain of a second doping type, a conduction channel of the first doping type, and a source including non-conducting means directly contacting the conduction channel and being contradoped for inherently providing a non-conducting response in the conduction channel to prevent a transistor effect from occurring between the drain and the source when predetermined voltages are applied to the first programmed cell to read the first programmed cell (claim 5, lines 1-10 of Fournel); wherein a region of the source not including the non-conducting means has a lower doping concentration than the drain (claim 6 of Fournel); and wherein the non-conducting means is the only region of the source that is contradoped (claim 5, lines 1-13 of Fournel).

In regards to claim 8, Fournel further discloses the non-conducting means is a first region of the source of the first programmed cell contradoped such that the first region is of the first doping type to form a degenerate transistor as the first programmed cell (claim 5, lines 1-10).

In regards to claim 9, Fournel differs from the claimed invention by not showing the first region of the source of the first programmed cell has a doping concentration less than that of the drain.

It would have been obvious to have the first region of the source of the first programmed cell has a doping concentration less than that of the drain because it depends on the desired threshold voltage of the transistor.

In regards to claim 10, Fournel discloses a method for programming a cell, comprising the steps of: forming, in a substrate of a first doping type, a first transistor having a drain of a second doping type, and a source of the second doping type at least a portion of which has a lower doping concentration than the drain, such that a portion of the substrate forms a conduction channel between the source and the drain; and contradoping only a first region of the source which directly contacts the conduction channel to make the first transistor degenerate (claims 11 and 12 of Fournel).

In regards to claim 11, Fournel further discloses the step of contradoping includes the step of: dividing the source into the first region, and a second region (claim 11, lines 15-22 of Fournel).

3. Applicant's arguments with respect to claims 1 and 3-12 have been considered but are moot in view of the new ground(s) of rejection.

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (571) 272-1657. The examiner can normally be reached on 8:20 am to 5:50 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sl
September 28, 2005

Steven Loke
Primary Examiner

Steven Loke